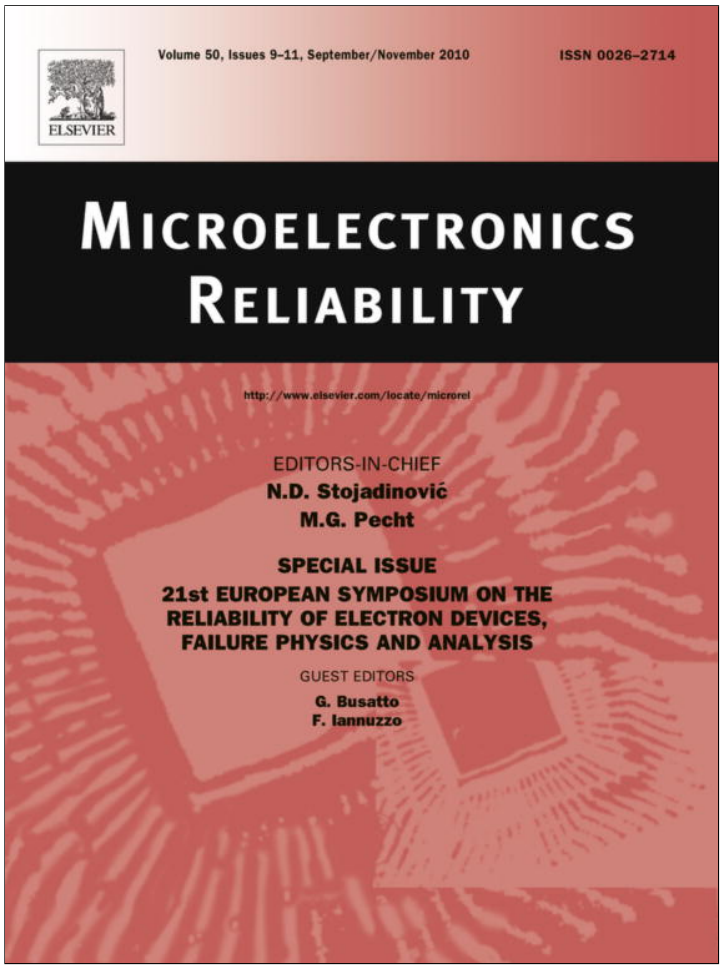

Microelectronics Reliability 50 (2010) 1528–1531

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Device reliability study of AlGaN/GaN high electron mobility transistors under high gate and channel electric fields via low frequency noise spectroscopy

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ARTICLE INFO

Article history:
Received 27 June 2010
Accepted 16 July 2010
Available online 16 August 2010

ABSTRACT

A set of different short term stress conditions are applied to AlGaN/GaN high electron mobility transistors and changes in the electronic behaviour of the gate stack and channel region are investigated by simultaneous gate and drain current low frequency noise measurements. Permanent degradation of gate current noise is observed during high gate reverse bias stress which is linked to defect creation in the gate edges. In the channel region a permanent degradation of drain noise is observed after a relatively high drain voltage stress in the ON-state. This is attributed to an increase in the trap density at the AlGaN/GaN interface under the gated part of the channel. It was found that self-heating alone does not cause any permanent degradation to the channel or gate stack. OFF-state stress also does not affect the gate stack or the channel.

1. Introduction

AlGaN/GaN based high electron mobility transistors (HEMTs) have shown excellent promise for high frequency and high power applications. A crucial technology challenge for its increased commercial success is its reliability [1]. Low frequency noise (LFN) has been known to be an extremely sensitive tool for studying early device degradation before actual breakdown takes place [2]. Although many reliability studies using low frequency noise measurements have been performed in AlGaN/GaN HEMTs [3–6] a simultaneous characterization of both gate and drain current noise is still unexplored. The latter gives the capability to study changes in the gate stack and channel region for a given stress condition and possible correlations [7].

This work demonstrates the results of a detailed investigation of simultaneous gate and drain current LFN characterization before and after high electric field and self-heating stress in the channel and gate stack.

A set of different stress conditions were applied to the device to isolate physical mechanisms viz. hot-carrier injection (HCI), inverse piezo-electric effect, self-heating effect and a combination of self-heating and HCI. The focus of this study has been limited to only short term stresses. In each case the noise was measured before and after stress respectively. A low bias (V_{DS} = 80 mV) transconductance measurement was also performed during and after stress.

2. Experimental setup and results

2.1. Device details

The devices under study are $Al_{0.26}Ga_{0.74}N$/GaN HEMTs grown on Si-substrate via metal organic chemical vapour deposition (MOCVD). AlN stress mitigation layers are employed to keep the defect densities in the GaN buffer layer to the minimum. Au/Ni is used as the gate Schottky contact and source and drain ohmic contacts are made of Au/Ti.

The device is passivated by silicon nitride and it has a source-connected field plate extension. The devices under study were mounted in a ceramic package eliminating exposure to light and varying ambient. More details of the device specification are presented in another work [7].

2.2. Experimental setup and stress methodology

An experimental setup was developed to perform automated electrical stressing, DC *I–V* characterization and drain and gate current LFN characterization (see Fig. 1). An Agilent E5252A is used to switch between a high power power supply unit (PSU) and a parameter analyser. For DC characterization, transconductance I_D–V_{GS} and I_G–V_{GS} were monitored. This was measured in the triode region at a low V_{DS} = 80 mV. LFN measurements were also performed in the triode regime of the HEMT via a 2-channel Agilent 35670A. The DC bias voltages were chosen in such a way that during noise measurements low currents (I_D < 25 mA) and low voltages (V_{DS} = 80 mV) are present in the device. Thus, the measurements were from a stress point of view electrically benign

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doi:10.1016/j.microrel.2010.07.073

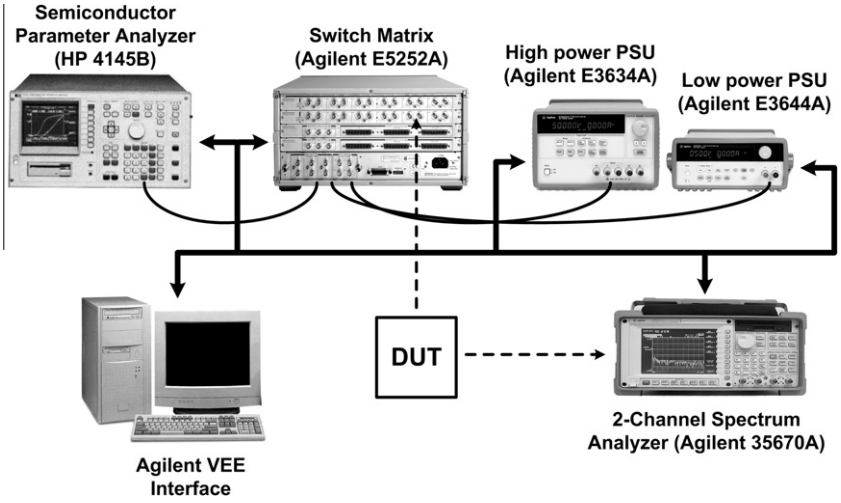

Fig. 1. Experimental setup for performing electrical stress and LFN characterization. The thick solid black lines show the GPIB connection to the computer. Thin solid lines show the electrical connections between instruments. Dashed arrow lines show the device connection to either noise setup (Agilent 35670A) or stress/*I*–*V* setup via a switch matrix (Agilent E5252A).

and non-destructive. The details of the noise measurement setup are presented in a separate paper [7].

Four different types of stress conditions were applied to the devices which are mapped to the typical I_D–V_{DS} load line DC biasing shown in Fig. 2. The four points invoke a combination of physical failure mechanisms like high self-heating ($P_D = I_D V_{DS}$), hot-carrier injection ($E_{CH} \sim V_{DS}$) and inverse piezo-electric effect. The four points can be expressed as four quadrants starting anti-clockwise from the top right.

Quadrant I: $V_{DS} = 20$ V at $V_{GS} = -1.7$ V, $I_{DS} = 0.115$ A/mm for 5 min. The device is stressed at constant voltage and channel current is monitored during stress.
Quadrant II: $V_{DS} = 2$ V at $V_{GS} = 2$ V, $I_{DS} = 0.2875$ A/mm for 30 min. Again, constant voltage is applied.
Quadrant III: $V_{DS} = 0$ V at $V_{GS} = 0$ to -20 V (-5 V increment), 10 min each step. Here, the constant voltage is stepped after 10 min of stressing.

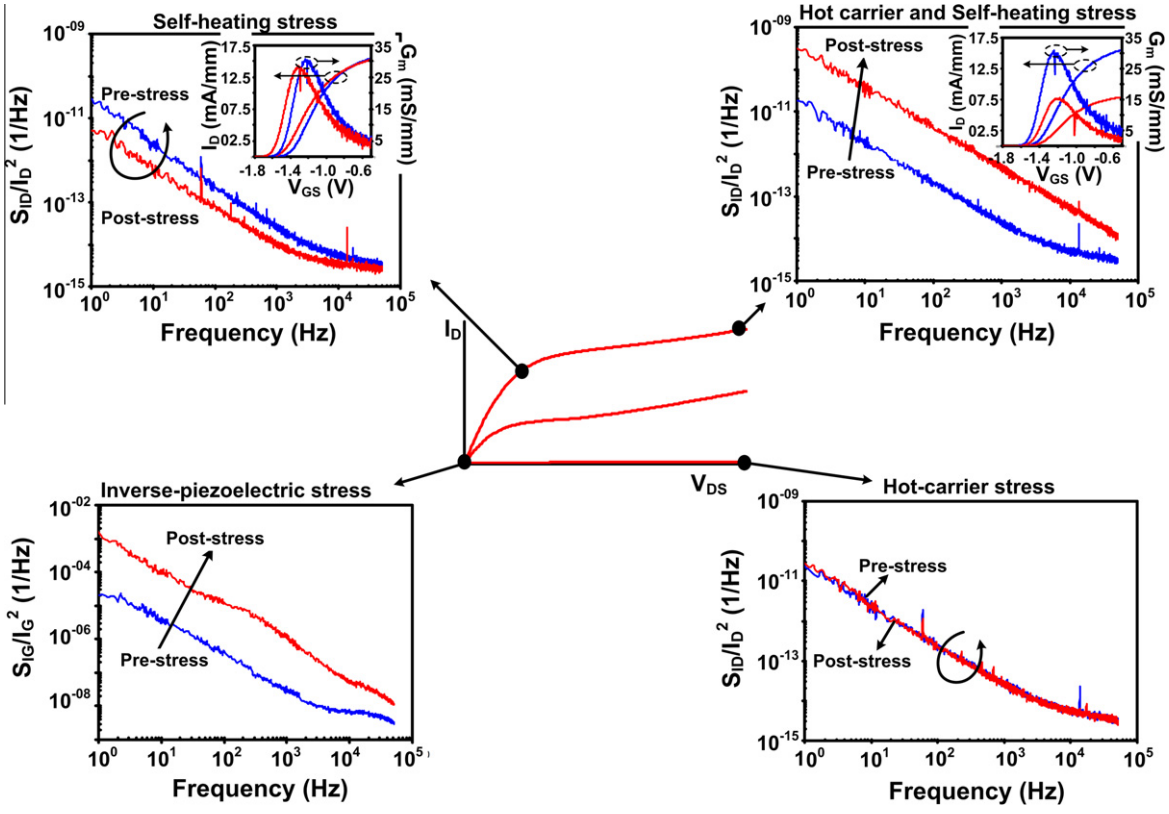

Fig. 2. Quadrants I, II and IV show pre- and post-stress normalized drain noise spectra (S_{ID}/I_D^2) in blue and red lines respectively. The insets in quadrants I and II are the transconductance and I_D–V_G in the linear region for pre- and post-stress (blue and red lines respectively). Quadrant III shows normalized gate noise spectra (S_{IG}/I_G^2) before and after stress.

Quadrant IV: V_{DS} = 10 to 30 V (5 V increment) at V_{GS} = −4 V. The channel current (I_{DS}) at 30 V stress was ~15 μA/mm. Here again, constant voltage is stepped after 20 min of stress.

Fig. 2 shows also the key changes in LFN in either drain or gate currents for each quadrant. Also shown is the corresponding change in the transconductance of the device in the triode region.

2.3. Results

The results indicate that there are two mechanisms at play. One is a transient effect like a threshold voltage shift due to electron trapping at deep levels in the AlGaN barrier layer during stress and detrapping subsequently. Second is a permanent change due to trap creation and/or migration which may lead to effects like permanent degradation of the low-field mobility and gate leakage currents. To isolate these phenomena, noise and DC measurements were carried up to several weeks after the stress procedures outlined above.

Quadrant I test conditions were equivalent to a high self-heating and hot-carrier injection environment for the device. It was observed that the drain current noise drastically degraded after the stress by almost one order of magnitude. This also resulted in a factor of two reduction in peak transconductance in the linear region. Both these changes were found to be permanent and did not show any recovery. It is interesting to point out here that right after stress, there was a positive shift in the threshold voltage of the device which later recovered to the pre-stress level. Therefore, this V_T shift was found to be a transient effect due to electron trapping and subsequently detrapping in existing trap states in the AlGaN barrier layer. By measuring channel noise as a function of gate bias it was determined that this degradation occurred in the gated part of the channel (Fig. 3). A Hooge parameter was calculated using the classical phenomenological equation,

$$\alpha_H = fN\left(\frac{S_{ID}^2}{I_D^2}\right) \quad (1)$$

The number of electrons in the channel (N) was determined by measuring the C–V characteristics of the gate-to-source/drain diode [7]. A Hooge parameter $\alpha_H = 1.5 \times 10^{-2}$ is calculated which is higher than the pre-stress α_H of ~10^{-3}. The gate current noise did not show any major changes in this regime. It is interesting to observe that such a large degradation can occur at such short duration. Most HCI related degradation mechanisms in these devices have shown relatively long time rates viz. few hours [8]. Therefore, hot-carriers alone cannot lead to this large degradation. The role of localized temperature increase leading to defect diffusion cannot be ruled out. This shows that effective control of channel temperature is imperative for obtaining increased reliability.

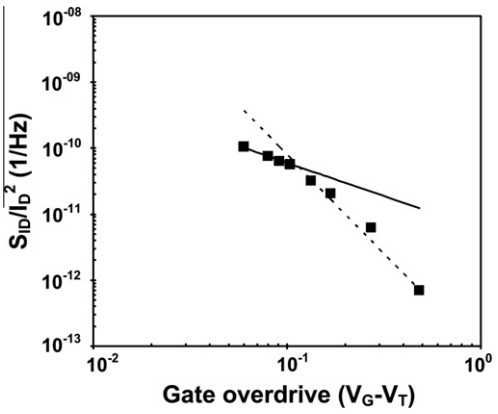

Fig. 3. Normalized drain current noise as a function of gate overdrive voltage. Square dots are the measured values. Solid and dashed lines are the V_G^{-1} and V_G^{-3} fits respectively. This dependence is a clear indicator of noise originating from the gated channel [7].

Quadrant II test conditions were predominantly self-heating effects and the drain noise characteristics showed a slight decrease due to the threshold voltage decrease. This later recovered to pre-stress levels when the threshold voltage recovered. It was concluded that no permanent degradation took place during this condition. The channel temperature is fairly uniform in this regime thus; most of the heat is spread out uniformly in the channel. It is therefore, not surprising that self-heating alone does not cause any degradation.

Quadrant III is a situation where only the gate stack was stressed since the source and drain are grounded. This has been shown to invoke high inverse-piezoelectric strain in the AlGaN barrier layer and no self-heating or hot-carriers in the channel [9]. It was found that post-stress gate current noise was severely degraded by almost one order. This change was permanent and did not recover even several weeks later. The drain noise exhibited transient changes due to threshold voltage shifts which later recovered once the stress was removed. Details about this stress condition are reported in another work [10].

The final quadrant (IV) stresses the device in the hot-carrier regime without self-heating. Threshold voltage shifts occurred during stress but no net shift occurred after stress. Both drain and gate noise characteristics did not show any post-stress change. Again no permanent degradation occurred in this regime. It seems that not enough hot-carriers were generated in the channel to cause changes.

3. Conclusions

A physical map of changes in the electronic behaviour of the device due to different stress vectors was deduced by performing simultaneous gate and drain current LFN characterization. An attempt was made to stress the device in a way so that only one physical effect dominates. The gate current noise degradation after high gate reverse bias stress show the first set of reported experimental results on trap creation under the gate stack due to inverse piezo-electric effect, a phenomenon extensively reported [9]. Hot-carrier injection combined with self -heating was also found to be a dominant cause of degradation in the channel for ON-state stress conditions by increasing the trap density at the AlGaN/GaN interface. This has also been reported before [1]. Finally, it was demonstrated that LFN measurements of both gate and drain currents are an excellent reliability characterization tool.

Acknowledgement

This work was supported by AFOSR MURI Grant No. FA9550-08-1-0264.

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